Patent claims

1. Method for identifying a data packet in a data stream in which
   - the d.c. voltage quota (dc) for a demodulated digital input signal (S_{in}) is calculated,
   - a k-bit word is allocated to the input signal (S_{in}), in that for each symbol of the input signal (S_{in}) corresponding to a bit a bit value (1 or 0) is determined as a function of the d.c. voltage quota (dc),
   - the k-bit word corresponding to the input signal(S_{in}) is compared with an expected k-bit synchronisation word in order to determine a correlation value (c_v) and
   - a packet identification signal (P_d) is generated if the correlation value (c_v) is greater than a correlation threshold value (c_{th}).

2. Method according to Claim 1, characterised in that for calculating the d.c. voltage quota (dc)
   - the input signal (S_{in}) is scanned in order to generate a sequence of scanned values (h_i) corresponding to the input signal (S_{in}) and
   - from a selected number (l) of scanned values (h_i) the d.c. voltage quota (dc) of the input signal (S_{in}) is calculated.

3. Method according to Claim 2, characterised in that the d.c. voltage quota (dc) of the input signal (S_{in}) is calculated again after each scan of the input signal (S_{in}) at least until the correlation value (c_v) determined by comparison of the k-bit word corresponding to the input

signal (S_{in}) with an expected k-bit synchronisation word is greater than the correlation threshold value (c_{th}).

4. Method according to Claim 2 or 3, characterised in that
   - after a packet identification signal (P_d) has been generated the corresponding correlation value (c_v) is stored and scanning of the input signal (S_{in}), calculation of the d.c. voltage quota (dc) and comparison of the k-bit word corresponding to the input signal (S_{in}) with an expected k-bit synchronisation word to determine the correlation value (c_v) is still continued for a predeterminable period of time and
   - a new packet identification signal (P_d) is generated if a newly determined correlation value (c_v) is greater than the correlation threshold value (c_{th}) and greater than the previously determined stored correlation value (c_v).

5. Method according to one of the preceding claims, characterised in that to determine the k-bit word corresponding to the input signal (S_{in})
   - the input signal (S_{in}) is scanned in order to generate a sequence of scanned values (h_i) corresponding to the input signal (S_{in}) and
   - a bit value (1 or 0) is allocated to each scanned value (h_i) of a selected multiplicity (k) of scanned values (h_i) as a function of the d.c. voltage quota (dc) of the input signal (S_{in}).

6. Method according to one of claims 1 to 5, characterised in that

- the input signal (S_{in}) is scanned at a frequency (f_{sample}) which is chosen in such a way that the over-scanning rate (s_r) is at least equal to two ($s_r \geq 2$), that therefore at least two scanned values (h_i) are determined for each symbol and
- to form the k-bit word corresponding to the input signal (S_{in}) in each case only one scanned value (h_i) per symbol is selected.

7. Method according to Claim 6, characterised in that the multiplicity (k) of scanned values (h_i) for forming the k-bit word corresponding to the input signal (S_{in}) is selected from the sequence of scanned values (h_i) in such a way that the selected scanned values (h_i) within the sequence in each case are substantially the same distance apart.

8. Method according to one of the preceding claims, characterised in that
   - the number (l) of scanned values (h_i) for calculating the d.c. voltage quota (dc) of the input signal (S_{in}) is chosen in such a way that the scanned values (h_i) correspond to areas in the expected k bit synchronisation word which substantially have the same number of bits with the value "0" and bits with the value "1" and
   - the d.c. voltage quota (dc) is calculated as an average value of the scanned values (h_i).

9. Method according to Claim 8, characterised in that the number (l) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of at least one group of

scanned values (h_i) in direct succession to one another, which correspond to several successive symbols.

10. Method according to Claim 8 or 9, characterised in that the number (l) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of two groups of scanned values (h_i), which are separated from one another by a multiplicity of scanned values (h_i).

11. Device for identifying data packets in a data receiving stream with
    - a delay line (22) which has a number (n) of storage places (22.i), in which scanned values (h_i) of a demodulated digital input signal (S_{in}) are stored in series,
    - a d.c. voltage quota determining circuit (30), which is connected to the delay line (22) in order to calculate a d.c. voltage quota (dc) of the input signal (S_{in}) as an average value of a selected number (l) of scanned values (h_i),
    - a decoding circuit (37) connected to the delay line (22) and the d.c. voltage quota determining circuit(30), which compares a multiplicity (k) of scanned values (h_i) with the d.c. voltage quota (dc) in order to allocate a bit value (0 or 1) to each scanned value (h_i) and in this way to form a k-bit word corresponding to the input signal (S_{in})
    - a comparison and correlation calculating circuit (41) which compares the k-bit word corresponding to the input signal (S_{in}) with an expected k-bit synchronisation word and calculates a correlation value

(c_v) for the k-bit word corresponding to the input signal (S_{in}) and

- a correlation value comparison circuit (43) which compares the correlation value (c_v) supplied by the comparison and correlation calculating circuit (41) with a correlation threshold value (c_{th}) in order to supply a packet identification signal (P_d) if the correlation value (c_v) is greater than or equal to the correlation threshold value (c_{th}).

12. Device according to Claim 11, characterised in that the number (n) of storage places (22.i) of the delay line (22) corresponds to the number (k) of bits in the k-bit synchronisation word multiplied by the over-scanning rate (s_r), in other words with the number of scanned values (h_i) per symbol.

13. Device according to Claim 11 or 12, characterised in that the decoding circuit (37) comprises a multiplicity (k) of comparison circuits, to which in each case is applied the d.c. voltage quota (dc) and each of which is connected to one of the storage places (22.i) of the delay line (22) in order to compare the respective scanned value (h_i) with the d.c. voltage quota (dc) and to determine a bit value (1 or 0), so the k-bit word corresponding to the input signal (S_{in}) is applied to outputs (out(i)) of the decoding circuit.

14. Device according to Claim 11, 12 or 13, characterised in that the d.c. voltage quota determining circuit (30) has at least one addition circuit (33) and one division

circuit (36) connected to the output of the addition circuit (33) via a holding element (34), wherein

- one input of the addition circuit (33) is connected to a first storage place ($22.m_1$, $22.m_3$) of the delay line (22) and another input is connected to a second storage place ($22.m_2$, $22.m_4$) of the delay line (22), which is separated from the first storage place ($22.m_1$, $22.m_3$) by a multiplicity of storage places (22.i),
- the input which is connected to the second storage place ($22.m_2$, $22.m_4$) is negated and
- the output of the addition circuit (33) is fed back to a third input via the holding element (34), so that with each addition the result of the preceding addition is added on and wherein
- the sum supplied by the holding circuit (34) is divided in the division circuit by a value ($m_1 - m_2$; $m_3 - m_4$) corresponding to the distance between the storage places ($22.m_1$, $22.m_3$; $22.m_2$, $22.m_4$) in order to calculate the d.c. voltage quota (dc).

15. Device according to Claim 14, characterised in that two addition circuits (33) connected to storage places ($22.m_1$, $22.m_3$; $22.m_2$, $22.m_4$) of the delay line (22) are provided, the output signals of which are supplied to the division circuit (36) via a further addition circuit (35).

16. Device according to one of the preceding claims, characterised in that the comparison and correlation calculating circuit (41) connected to the decoding circuit (37) and a register (42) storing the expected k-bit synchronisation word, besides a multiplicity (k) of comparison circuits for comparing the k-bit word supplied

by the decoding circuit (37) and corresponding to the input signal with the k-bit synchronisation word, has a correlation element which adds a one for each coinciding bit pair in order to calculate the correlation value (c_V).